REMARKS

Claims 1- 23 are pending. Claim 1 has been amended herein. No no new matter has been added as a result of this amendment. One corrected drawing sheet labeled "Replacement Sheet" in the page header has been provided.

Drawings

In the amended Figure 2, the previously omitted element numeral 61 has been added. A replacement sheet, labeled "Replacement Sheet" is attached.

§102 Rejections

Claims 1, 3 – 4, and 6 – 23 are rejected under 35 U.S.C. §102(e), as being anticipated by Gibson et al. U.S. Patent No. 6,601,167 (hereinafter, Gibson). Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claims 1, 3 – 4, and 6 – 23 is neither shown nor suggested by Gibson.

Examiner is respectfully directed to independent Claim 1, which recites that an embodiment of the present invention is directed to, a non-volatile memory that comprises:

> A SDRAM style memory interface, wherein said SDRAM style memory interface requires initialization prior to use;
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> SDRAM style address lines multiplexed in time, wherein a least significant portion and a most significant portion of an address are presented sequentially in two successive stages; and
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> SDRAM style sequential access logic incorporated in a logic subsystem, such that after a first address sequence is presented a second and subsequent

address locations can be read using one or more additional SDRAM style control signals.

Applicant submits that Gibson does not anticipate or render obvious, a non-volatile memory that has a SDRAM style memory interface, as is recited in Claim 1. Therefore, Claim 1 is not anticipated. A non-volatile memory with an SDRAM style memory interface, address lines, and sequential access logic, as claimed in Claim 1, can be controlled with existing non-unique addressing signals, and does not require unique sequential logic control signals when used in a system designed to use SDRAM devices. Gibson discloses a sequential access memory. See e.g. col. 2, lines 23-24. However, Gibson teaches away from Claim 1, by further disclosing that the sequential access memory is an UltraNAND memory, and that system applications using it must generate the proper control signals for the device, which, in many cases, are not used by any other system resource. See e.g., col. 7, Lines 9 – 23 and col. 8, lines 9 – 55. Accordingly, applicant submits that Gibson does not teach or suggest, either expressly or inherently, a non-volatile memory that comprises "a SDRAM style memory interface," as is recited in Claim 1.

Therefore, Applicant respectfully submits that Gibson fails to anticipate or render obvious the Applicant's invention as is set forth in Claim 1, and as such, Claim 1 traverses the Examiner's basis for rejection under 35 U.S.C. 102(e) and is in condition for allowance.

Examiner is respectfully directed to independent Claim 3, which recites that embodiments of the current invention are directed to a method of initializing a computer system, comprising:

> ... reading a boot code stored in a non-volatile memory, wherein the memory has a SDRAM style interface, and wherein the first memory location in the non-volatile memory is read using at least one control signal that functions independently of the SDRAM style interface.

Claim 4 depends from independent Claim 3 and recites a further limitation of the claimed invention.

Applicant submits that Gibson does not anticipate or render obvious a method of initializing a computer system comprising, "reading a boot code stored in a non-volatile memory, wherein the memory has a SDRAM style interface, and wherein the first memory location in the non-volatile memory is read using at least one control signal that functions independently of the SDRAM style interface," as is recited in Claim 3. Therefore, Claim 3 is not anticipated. Gibson teaches a non-volatile memory having certain interface requirement for boot access, such as utilizing a multi-plexed address/data bus, wherein all command, address, and data information is passed to and from the device through an eight bit input output port. See e.g., col. 7, lines 9-12. Gibson teaches that bootstrap loading is accomplished by initiating a read command to the memory and then providing an address into an address latch. See e.g., col. 3, lines 52-59. Gibson also teaches a memory that must be initialized before code can be fetched sequentially out of its registers. See e.g. col. 11, lines 15 -17. Gibson also teaches that it is possible to use a series of move immediate instructions in order to assemble the second portion of boot code into memory. See e.g., col 5, lines 42 – 44 and col. 11, lines 40 – 65. However, Gibson does not teach or suggest, either expressly or inherently, a memory having an SDRAM style memory interface, as recited in Claim 3. Further, Gibson does not teach or suggest, either expressly or inherently "reading a boot code stored in a non-volatile memory, wherein the memory has a SDRAM style interface, and wherein the first memory location in the non-volatile memory is

read using at least one control signal that functions independently of the SDRAM style interface," as recited in Claim 3.

Therefore, Applicant respectfully submits that Gibson fails to anticipate or render obvious the Applicant's invention as is set forth in Claim 3, and as such, Claim 3 traverses the Examiner's basis for rejection under 35 U.S.C. 102(e) and is in condition for allowance. Accordingly the Applicant also respectfully submits that Gibson does not anticipate or render obvious the present claimed invention as is recited in Claim 4 dependent on Claim 3, and that this Claim overcomes the rejection under 35 U.S.C. 102(e) through dependency on an allowable base claim.

Examiner is respectfully directed to independent Claim 6, which recites that embodiments of the present invention are directed to a method of configuring a SDRAM interface in a computer system wherein the computer system has an non-volatile memory with a SDRAM style interface, comprising:

> ...providing at least one control signal independent of the SDRAM style interface for performing a read operation from the first location in the first accessed memory row of the non-volatile memory, and
>
> providing a least one control signal independent of the SDRAM style interface for incrementing the internal address of the non-volatile memory.

Claims 7 - 9 depend from independent Claim 6 and recite further limitations of the claimed invention.

Applicant submits that Gibson does not anticipate or render obvious a method of configuring a SDRAM interface in a computer system wherein the computer system has an non-

volatile memory with a SDRAM style interface comprising, "providing at least one control signal independent of the SDRAM style interface for performing a read operation from the first location in the first accessed memory row of the non-volatile memory," as is recited in Claim 6. Therefore, Claim 6 is not anticipated. The Gibson reference teaches a sequential access memory and a boot loader that controls the sequential access memory. See col. 14, lines 37 – 41, and col. 2, lines 22 – 29. However, Gibson does not teach or suggest, either expressly or inherently, a non-volatile sequential access memory having an SDRAM style interface, as recited in Claim 6. Further, Gibson does not teach or suggest, either expressly or inherently, "providing at least one control signal independent of the SDRAM style interface for performing a read operation from the first location in the first accessed memory row of the non-volatile memory," as is recited in Claim 6.

Therefore, Applicant respectfully submits that Gibson fails to anticipate or render obvious the Applicant's invention as is set forth in Claim 6, and as such, Claim 6 traverses the Examiner's basis for rejection under 35 U.S.C. 102(e) and is in condition for allowance. Accordingly the Applicant also respectfully submits that Gibson does not anticipate or render obvious the present claimed invention as is recited in Claims 7 - 9 dependent on Claim 6, and that these Claims overcome the rejection under 35 U.S.C. 102(e) through dependency on an allowable base claim.

Examiner is respectfully directed to independent Claim 10, which recites that embodiments of the present invention are directed to a computer system comprising: "non-volatile memory, and volatile memory, wherein the non-volatile memory and volatile memory

have a common interface." Claims 11 - 19 depend from independent Claim 10 and recite further limitations of the claimed invention.

Applicant submits that Gibson does not anticipate or render obvious a computer system comprising "non-volatile memory, and volatile memory, wherein the non-volatile memory and volatile memory have a common interface," as is recited in Claim 10. Therefore, Claim 10 is not anticipated. Gibson teaches a sequential access memory that can transfer data to a Random Access Memory. See col. 2, lines 6 -10. However, Gibson does not teach or suggest, either expressly or inherently, "non-volatile memory, and volatile memory, wherein the non-volatile memory and volatile memory have a common interface," as is recited in Claim 10. In fact, the cited reference from Gibson teaches away from this by teaching two kinds of non-volatile memory that have different interfaces: one which requires a setup and prior to use; and one that does not. See col.2, lines 6–10. Having two kinds of non-volatile memory with two separate interfaces precludes having a computer system comprising "non-volatile memory, and volatile memory, wherein the non-volatile memory and volatile memory have a common interface," as recited in Claim 10.

Therefore, Applicant respectfully submits that Gibson fails to anticipate or render obvious the Applicant's invention as is set forth in Claim 10, and as such, Claim 10 traverses the Examiner's basis for rejection under 35 U.S.C. 102(e) and is in condition for allowance. Accordingly the Applicant also respectfully submits that Gibson does not anticipate or render obvious the present claimed invention as is recited in Claims 11 - 19 dependent on Claim 10, and that these Claims overcome the rejection under 35 U.S.C. 102(e) through dependency on an allowable base claim.

Examiner is respectfully directed to independent Claim 20, which recites that embodiments of the present invention are directed to a computer system comprising "a non-volatile memory having a SDRAM style interface." Claims 21 - 23 depend from independent Claim 20 and recite further limitations of the claimed invention.

Applicant submits that Gibson does not anticipate or render obvious a computer system comprising "a non-volatile memory having a SDRAM style interface." as is recited in Claim 20. Therefore, Claim 20 is not anticipated. Gibson teaches a sequential access memory and a boot loader that controls the sequential access memory. See col. 14, lines 37 – 41, and col. 2, lines 22 – 29. However, Gibson does not teach or suggest, either expressly or inherently, "a non-volatile sequential access memory having an SDRAM style interface," as recited in Claim 20.

Therefore, Applicant respectfully submits that Gibson fails to anticipate or render obvious the Applicant's invention as is set forth in Claim 20, and as such, Claim 20 traverses the Examiner's basis for rejection under 35 U.S.C. 102(e) and is in condition for allowance. Accordingly the Applicant also respectfully submits that Gibson does not anticipate or render obvious the present claimed invention as is recited in Claims 21 - 23 dependent on Claim 20, and that these Claims overcome the rejection under 35 U.S.C. 102(e) through dependency on an allowable base claim.

Claim 2 is rejected under 35 U.S.C. §102(e), as being anticipated by Zarrin et al. U.S. Patent No. 6,128,731 (hereinafter, Zarrin). Applicant has reviewed the cited reference and

respectfully submits that the present invention as recited in Claim 2 is neither shown nor suggested by Zarrin.

Examiner is respectfully directed to independent Claim 2, which recites that an embodiment of the present invention is directed to "a computer system that includes non-volatile memory and SDRAM, wherein the non-volatile memory shares a common interface with SDRAM."

Applicant submits that Zarrin does not anticipate or render obvious "a computer system that includes non-volatile memory and SDRAM, wherein the non-volatile memory shares a common interface with SDRAM," as is recited in Claim 2. Therefore, Claim 2 is not anticipated. Zarrin teaches a processor coupled to a volatile memory and a non-volatile memory via one or more buses. A bus is only part of an SDRAM interface, not a complete interface. However, Zarrin does not teach or suggest, either expressly or inherently, "a computer system that includes non-volatile memory and SDRAM, wherein the non-volatile memory shares a common interface with SDRAM," as recited in Claim 2.

Therefore, Applicant respectfully submits that Zarrin fails to anticipate or render obvious the Applicant's invention as is set forth in Claim 2, and as such, Claim 2 traverses the Examiner's basis for rejection under 35 U.S.C. 102(e) and is in condition for allowance.

Claim 5 is rejected under 35 U.S.C. §102(e), as being anticipated by Wisor, U.S. Patent No. 6,823,435 (hereinafter, Wisor). Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claim 2 is neither shown nor suggested by Wisor.

Examiner is respectfully directed to independent Claim 5, which recites that an embodiment of the present invention is directed to a method of reducing control lines and address lines in a computer system having non-volatile memory, comprising "providing the non-volatile memory with a SDRAM style interface."

Applicant submits that Wisor does not anticipate or render obvious "providing the non-volatile memory with a SDRAM style interface," as is recited in Claim 5. Therefore, Claim 5 is not anticipated. Wisor teaches a non-volatile memory system having a programmably selectable boot code section size. Wisor also teaches accessing the internal memory cells of a memory array using address signals driven upon the address lines of a memory bus. However, Wisor does not teach or suggest, either expressly or inherently "providing the non-volatile memory with a SDRAM style interface," as recited in Claim 5.

Therefore, Applicant respectfully submits that Wisor fails to anticipate or render obvious the Applicant's invention as is set forth in Claim 5, and as such, Claim 5 traverses the Examiner's basis for rejection under 35 U.S.C. 102(e) and is in condition for allowance.

SUMMARY

In view of the foregoing remarks, the Applicant respectfully submits that the pending claims are in condition for allowance. The Applicant respectfully requests reconsideration of the Application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Jeffery B. Morris at (408) 938-9060.

Respectfully submitted,
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Dated: 8 Apr, 2005

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AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 2. This sheet replaces the original sheet that included Fig. 2. In the replacement sheet containing Figure 2, previously omitted element 61 has been added.

Attachment: Replacement Sheet, annotated showing changes